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U.S. UTILITY Patent Application

PATENT NUMBER and ISSUE DATE

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10076458	02/19/2002	324	501	2858	TURESSON

**APPLICANTS: Tsuji Yoshio; Yamada Masayoshi;

**CONTINUING DATA VERIFIED: NONE JT

** FOREIGN APPLICATIONS VERIFIED: JT

JAPAN 2001-42356 02/19/2001

JAPAN 2001-111132 04/10/2001

JAPAN 2001-111133 04/10/2001

PG-PUB	DO NOT PUBLISH ☐	RESCIND ☐	
Foreign priority claimed	☒ yes ☐ no		ATTORNEY DOCKET NO
35 USC 119 conditions met	☒ yes ☐ no		
Verified and Acknowledged Examiners's intials	JT		0052/064001

TITLE : Circuit board testing apparatus and method for testing a circuit board

U.S.DEPT. OF COMM./PAT.& TM-PTO-436L(Rev. 12-94)

NOTICE OF ALLOWANCE MAILED			CLAIMS ALLOWED	
	Assistant Examiner		Total Claims	Print Claim for O.G.
ISSUE FEE			DRAWING	
Amount Due / Date Paid			Sheets Drwg. / Figs.Drwg. / Print Fig.	
	Primary Examiner			
☐ TERMINAL DISCLAIMER	PREPARED FOR ISSUE		Application Examiner	

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